CpE Lab

Lab 3: Field Programmable Gate Arrays

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Introduction

The focus of this lab was to introduce FPGAs, their characteristics and uses, and also to teach students how to design and program circuits using Quartus II. This lab also introduced students to DE2 boards and some of its components.

Part I

Experiment

The objective of this experiment is to design a circuit using the Quartus II program and to verify its truth table. The circuit to be designed and its truth table are shown below:



Figure 1

Methodology

The first approach taken to solve this problem was to launch Quartus II, start a new project and fill out all the required information like the name and the directory of the project. The next step taken was to select the name of device family and the device name which were Cyclone II and EP2C35F672C6 respectively.

The group then designed the circuit in figure 1 on the graphic editor window, using two 2-input AND gates, one 2-input OR gate, two 2-input NOT gates, two inputs and one output. This was achieved by importing logic gate symbols and input and output symbols unto the editor window, and arranging them in such a way as to exactly resemble the circuit depicted above in figure 9. Importing the logic gate and input and output symbols was an easy task. It was done by clicking on the blank space on the editor window and selecting the required logic gates from the pop up box. The final step in designing the circuit was to name the two inputs respectively and the output .

After this the group proceeded to compile the designed circuit. This was done by selecting the “start compilation” option found under the “processing” tab. Next the group assigned input to pin N25, input to pin N26 and the output to pin AE22 of the DE2 board. This was done by following the instructions made available in the lab handout. The group then recompiled the circuit so that the pins would be assigned properly. The group programmed and configured the FPGA device by following the instructions under the “programming and configuring the FPGA device” section in the lab handout, and next proceeded to test the circuit.

Result

The green LED (pin AE22 on the DE2 board) lit up only when one input was high and the other one low, thus verifying the truth table.

Part II

Experiment I: Half Adder

The goal of this part of the lab is to determine the truth table, logic expression and schematics for a Half Adder circuits, and to design and program it on Quartus II.

Methodology

To determine the truth table for the half adder circuit, the group based its prediction on the knowledge that the half adder was simply a circuit capable of adding two single-bit binary numbers; hence it should be able to execute the following operations: 0+0, 0+1, 1+0 and 1+1 all in binary. After realizing this, the group was able to write the truth table by having two inputs with four possible operations (which were mentioned above) and two outputs named carry and sum respectively which represented the two bit results of the operations.

Next the group wrote the logic expression for both the carry and sum output. This was an easy task to achieve as the group deduced that the truth table excluding the sum output resembled that of an AND gate, while the truth table excluding the carry output resembled the truth table of an XOR gate.

Lastly the group sketched the schematics of the Half Adder circuit and designed and programmed it using Quartus II. This was done by following the methods learned in experiment I for designing and programming a circuit. The group made its prediction on how the circuit would look like based on the fact that the logic expression shows that there are two inputs and outputs, an AND gate and an XOR gate. The output of the XOR gate was named Sum, and the output of the AND gate was named Carry. Also the two inputs were assigned to switches 0 and 1, and the outputs were connected to LEDs.

Results

The results obtained are presented below in the form of a logic expression, a truth table and the schematic for the circuit.

Logic Expression:

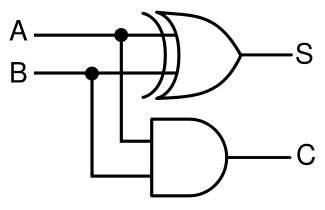
Carry

Sum

Truth Table:

|  |  |  |  |
| --- | --- | --- | --- |
| Input x | Input y |  | Sum |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The circuit design:



Experiment II: Full Adder

The goal of this part of the lab is to determine the truth table, logic expression and schematics for a Full Adder circuits, and to design and program it on Quartus II.

Methodology

The group predicted that the full adder would be made up of two half adder circuits and probably something else (maybe a gate) because unlike the half adder, it can perform eight operations. After pondering on the design of the circuit, the group made the assumption that the “something else” required was an OR gate, and the predicted schematics for the circuit was then sketched out on the lab handout. Next the design was imported unto the editor board on Quartus II, and the inputs and outputs were assigned to the same pins used when designing the half adder circuit, with the exception of the new input which was assigned to pin P25. The final step was to compile, program and test the circuit

Results The results obtained are presented below in the form of a logic expression, a truth table and the schematic for the circuit.

Logic Expression

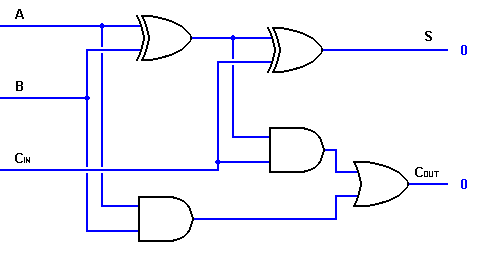
Sum= (

Carry-(

Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input x | Input y |  | Carryout | Sum |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

The circuit design



Lab 3 Post Lab Questions

) They are: N25, N26, P25, AE14, AF14, AD13 and AC13

) 9v

Lab 4 Pre Lab Questions

Q1) Very high speed integrated Hardware Design Language

Q2) Cyclone II, EP2C35F672C6, and any respectively.